REMARKS/ARGUMENTS

1. Objection to claims 1, 2, 4, 6, 7, and 9:

Claims 1, 2, 4, 6, 7, and 9 are objected to under 37 CFR 1.75(a) because "R", "M", and "N" just be defined in the claims, e.g., wherein the first coefficient R is a natural number.

Response:

Claims 1 and 6 have been amended to specify that the coefficients "R", "M", and "N" are all natural numbers. Acceptance of the claims is respectfully requested.

2. Rejection of claims 1-10 under 35 U.S.C. 103(a):

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art, hereinafter AAPA.

Response:

Independent claims 1 and 6 have been amended to overcome these rejections. The limitations of claims 2, 4, and 5 have been added to claim 1, and the limitations of claims 7, 9, and 10 have been added to claim 6. In addition, each of the independent claims also contains the step of recording values of the first coefficients R, the second coefficients M, the third coefficients N, and the minimum difference for each loop operation. These amendments are fully supported in the specification and in Figure 3, and no new matter has been introduced as a result of these amendments to claims 1 and 6. In addition, paragraphs [0015] and [0016] of the specification have been amended to reflect the amendments made to claims 1 and 6.

Unlike the AAPA, the present invention according to claims 1 and 6 calculates differences between the calculated quotients and the predetermined pixel clock, and

in subsequent loop operations, compares the previously calculated difference with new calculated difference to obtain a minimum difference. Values of the first coefficients M, the second coefficients N, the third coefficients R, and the minimum difference are then recorded for each loop operation. Finally, after all of the loop operations are executed, the smallest difference is identified, and the actual pixel clock is generated according to the quotient associated with the minimum difference.

In contrast, the prior art teaches comparing calculated clocks CLKcal to the optimum clock CLKbest that was previously calculated. For each loop of the operation, values of the first coefficients M, the second coefficients N, the third coefficients R, and the optimum clock CLKbest difference are recorded. The differences in memory usage between the prior art method and the claimed method is explained below.

If the loop operations involve using three embedded loops, with each of the three loops going through 128 iterations, then a total of 128*128*128 loop operations are needed. As explained in paragraphs [0048] and [0049] of the specification, since only the minimum difference DIFF is recorded instead of the value of the calculated clock CLKcal, less memory is needed to store the results of each loop operation. This leaves more room for the BIOS of the display driving circuit to store other program codes, and solves other memory problems caused the large memory requirements of the prior art.

For these reasons, the claimed invention provides significant memory savings over the prior art, and the applicant submits that the limitations of claims 1 and 6 are not obvious over the prior art. Furthermore, claims 3 and 8 are dependent on claims 1 and 6, and should be allowed if claims 1 and 6 are allowed. Reconsideration of claims 1, 3, 6, and 8 is therefore respectfully requested. Applicant respectfully

requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: 11/15/2006

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)